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10/25/02

PATENT
2207/9865

2185

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	:	Manoj KHARE et al.
SERIAL NO.	:	09/749,660
FILING DATE	:	12/28/2000
GROUP ART UNIT	:	2185
FOR	:	METHOD AND APPARATUS FOR REDUCING MEMORY LATENCY IN A CACHE COHERENT MULTI-NODE ARCHITECTURE
EXAMINER	:	Unknown

Commissioner of Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97

S I R:

In accordance with Applicant's duty of disclosure under 37 C.F.R. §1.56(a) and §1.97(c), the references listed on the attached form PTO-1449 are hereby brought to the Examiner's attention. Copies of the references are enclosed. These references were uncovered through a keyword computer search.

It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear in the "references cited" on any patent to issue therefrom.

Respectfully submitted,

KENYON & KENYON

Date: February 25, 2002

By: _____
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CERTIFICATE OF MAILING

I hereby certify that the following documents are being deposited with the United States Postal Service as First Class Mail in a large envelope addressed to: Assistant Commissioner for Patents, Box IDS, Washington, DC 20231, marked "1 of 3", with regard to Docket No. 2207/9865, Serial No. 09/749,660

1. Information Disclosure Statement Under 37 C.F.R. 1.97
2. Copies of All References Listed on IDS
3. Postcard

Dated: February 25, 2002

KENYON & KENYON

By: Pilar Rodriguez
Pilar M. Rodriguez